STANSON

STN2018 Lead-free

N Channel Enhancement Mode MOSFET

10.0A

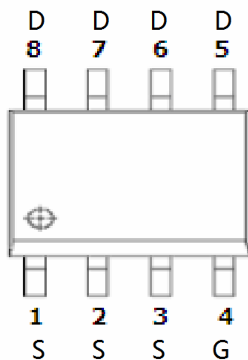
DESCRIPTION

STN2018 is the N-Channel logic enhancement mode power field effect transistors which are produced using high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application, notbook computer power management and other battery powered circuits where high-side switching.

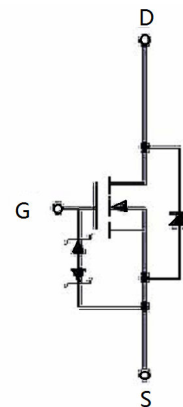
PIN CONFIGURATION

SOP-8



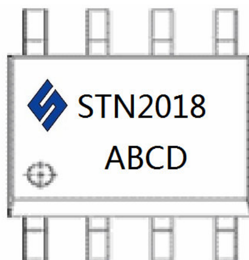
FEATURE

- 20V/10A, $R_{DS(ON)}$ = 10mΩ @VGS = 4.5V
- 20V/7A, $R_{DS(ON)}$ = 15mΩ @VGS = 2.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP-8 package design



PART MARKING

SOP-8



A : Year B : Date Code

C : Manufacture D : Wafer Lot

STANSON TECHNOLOGY
120 Bentley Square, Mountain View, Ca 94040 USA
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ABSOULTE MAXIMUM RATINGS (Ta = 25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	20	V
Gate-Source Voltage		V_{GSS}	±12	V
Continuous Drain Current (TJ=150℃)	T_A=25℃ T_A=70℃	I_D	10.0 8.0	A
Pulsed Drain Current		I_{DM}	35	A
Continuous Source Current (Diode Conduction)		I_S	2.3	A
Power Dissipation	T_A=25℃ T_A=70℃	P_D	2.5 1.6	W
Operation Junction Temperature		T_J	-55/150	℃
Storgae Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	80	℃/W

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ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250 uA	0.6		1.4	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±12V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=20VV_{GS}=0V			1	uA
	T_J=55℃	V_{DS}=20VV_{GS}=0V			10	uA
On-State Drain Current	$I_{D(on)}$	V_{DS}≥5V,V_{GS}=4.5	6			A
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=4.5V, I_D=10A V_{GS}=2.5V, I_D=7.0A		0.008 0.011	0.012 0.015	Ω
Forward Tran Conductance	g_{fs}	V_{DS}=15.0V,I_D=5.0A		30		S
Diode Forward Voltage	V_{SD}	I_S=1.0A,V_{GS}=0V		0.8	1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=10V,V_{GS}=4.5V I_D=5.0A		18	25	nC
Gate-Source Charge	Q_{gs}			4.2		
Gate-Drain Charge	Q_{gd}			6.8		
Input Capacitance	Ciss	VDS=10V,VGS=0V f=1MHz		850		pF
Output Capacitance	Coss			135		
Reverse TransferCapacitance	Crss			105		
Turn-On Time	$t_{d(on)}$	V_{DD}=10V,R_L=10Ω I_D=1.0A,V_{GEN}=4.5V R_G=6Ω		12	16	nS
	t_r			10	28	
Turn-Off Time	$t_{d(off)}$			30	55	
	t_f			35	58	

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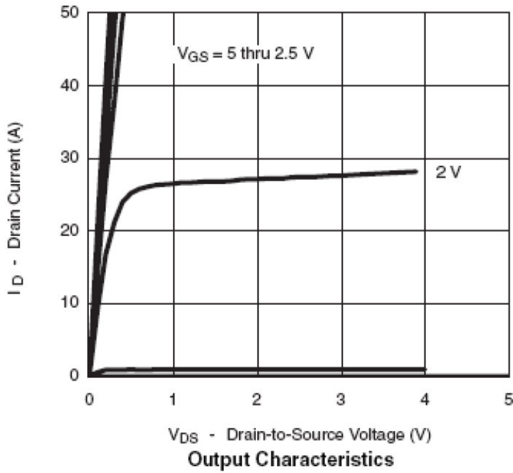
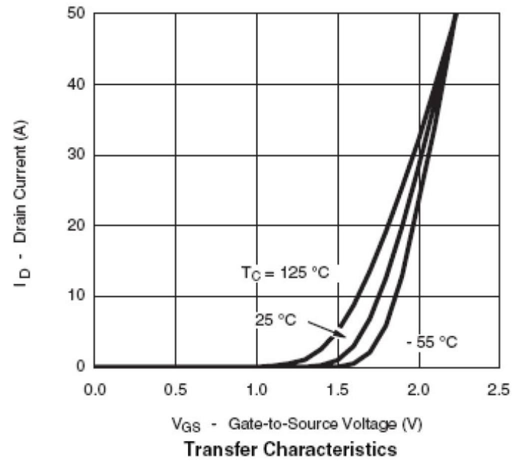
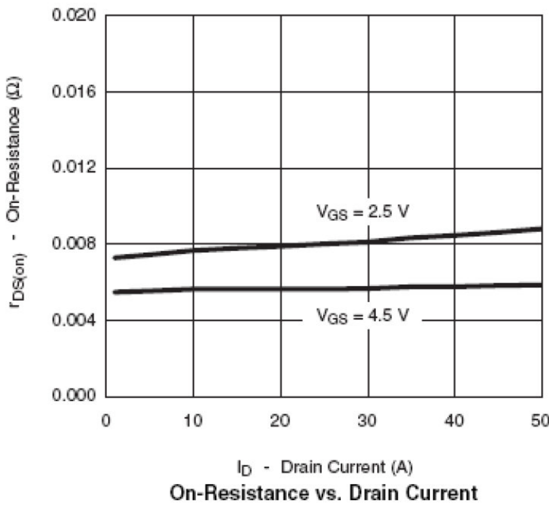
TYPICAL CHARACTERICTICS (25℃ Unless Note)



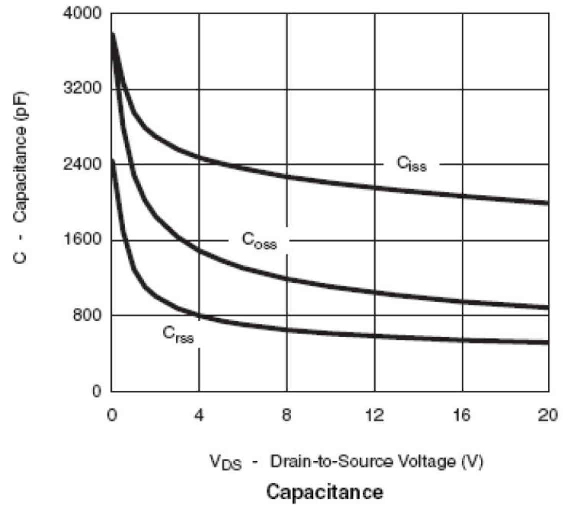
Output Characteristics



Transfer Characteristics



On-Resistance vs. Drain Current



Capacitance

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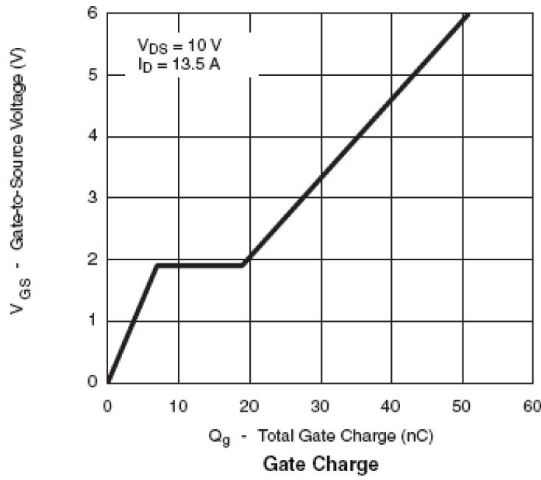
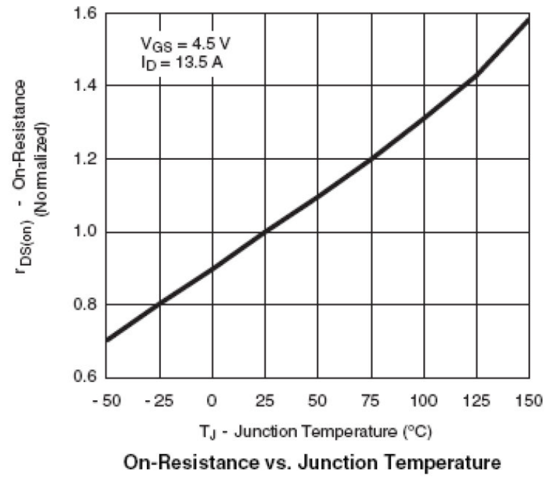
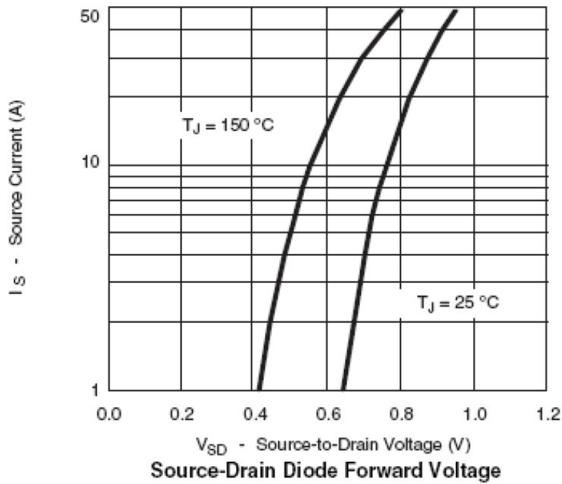


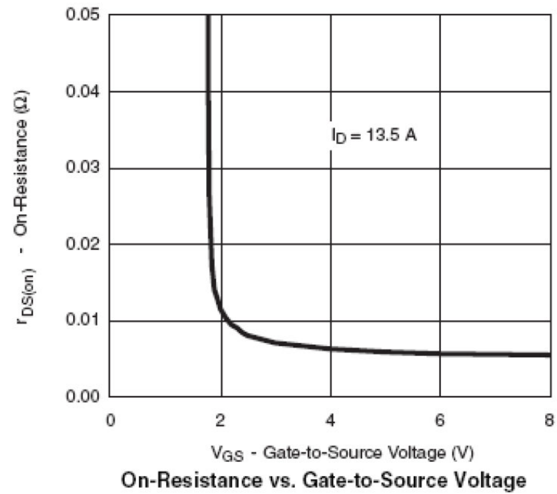
Gate Charge



On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

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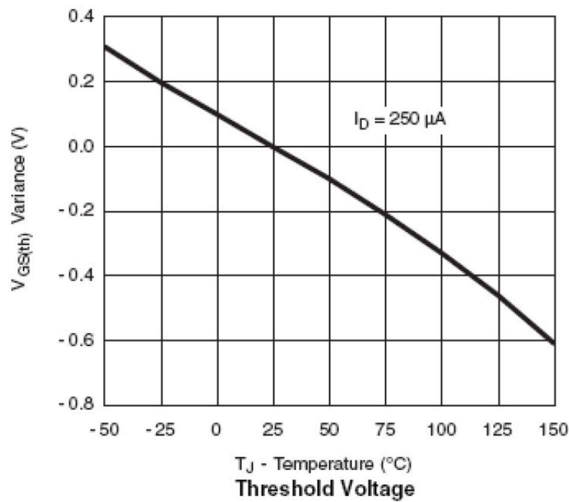
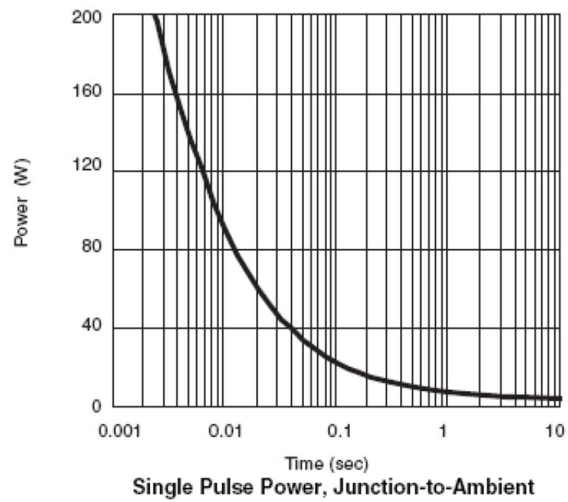
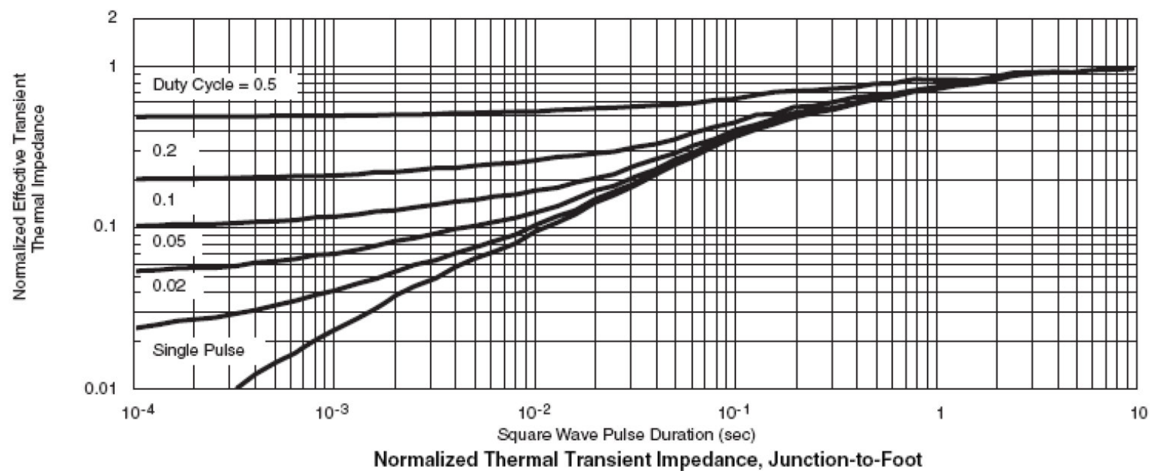


Threshold Voltage



Single Pulse Power, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

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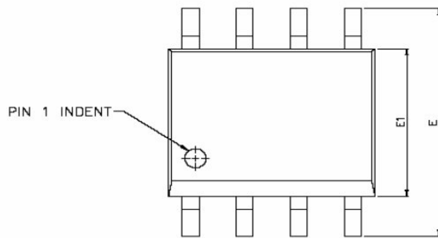
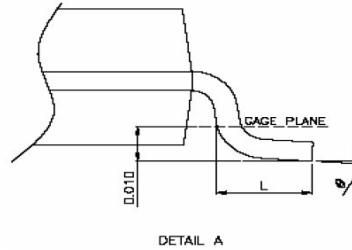
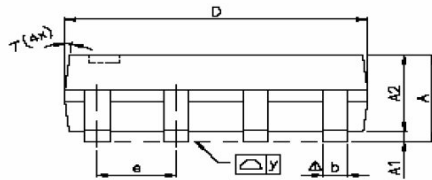
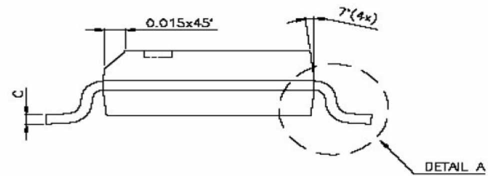
SOP-8 PACKAGE OUTLINE









SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	——	0.25	0.004	——	0.010
A2	——	1.45	——	——	0.057	——
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	——	1.27	——	——	0.050	——
L	0.38	0.71	1.27	0.015	0.028	0.050
⚠2 y	——	——	0.076	——	——	0.003
θ	0°	——	8°	0°	——	8°

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